## REMARKS

The last Office Action in the above-identified application and the references cited by the Examiner have been carefully considered. Claims 1 and 3 have been amended in a sincere effort to define more clearly and more specifically features of Applicant's invention which distinguish over the art of record.

Claim 1 has been rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 5,708,284 (Onishi). The Examiner contends that the Onishi patent discloses an insulation film 7 having a concave portion at a top surface, a laminated body obtained by laminating a plurality of layers on the top surface and etching a region of the plurality of layers corresponding to a region other than the concave portion, where the laminated body includes a lower electrode 8 which is brought into contact with a bottom surface of the concave portion, a ferroelectric layer 9 formed on the lower electrode 8 and an upper electrode layer 10 formed on the ferroelectric layer 9, where a portion of the lower electrode layer 8 protrudes outward from an inner peripheral edge forming the concave portion, and a side of a portion of the lower electrode layer 8, a side of the ferroelectric layer 9, and a side of the upper electrode layer 10 are flush with each other (the Examiner refers to Figure 6 of the Onishi patent for showing this structure), and a film 8a formed in a bottom of the hollow and separating between the insulating film 7 and the lower electrode layer 8b (the Examiner again refers to Figure 6 of the Onishi patent for showing this structure).

Claim 2 has also been rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,344,413 (Zurcher, et al.). The rejection of Claim 2 in view of the Zurcher, et al. [illegible] herein, as Claim 2 has now been cancelled.

Claim 3 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over the Onishi patent in view of U.S. Patent 5,861,344 (Roberts, et al.), which has been newly cited in this case. The Examiner, basically, states that the Onishi patent discloses the structure mentioned previously with respect to Claim 1, but acknowledges that the Onishi patent fails to disclose that the first electrode portion 8a is formed only at a corner of the hollow. The Examiner, however, contends that the Roberts, et al. patent discloses forming an improved electrical contact by depositing the corner fill 32 in the hollow, and refers to Column 7, lines 19-30 and Figures 3 and 4 of the Roberts, et al. patent for disclosing this. The Examiner further contends that the Roberts, et al. patent discloses that the first electrode portion acts as seeding material and selective deposit at the corner, and refers to Column 2, lines 41-44 of the Roberts, et al. patent for disclosing this, and further contends that the Roberts, et al. patent teaches that this improves metal contact in the hollow, at Column 7, lines 19-23 thereof. The Examiner concludes, therefore, that it would have been obvious for one with ordinary skill in the art to modify the Onishi structure in accordance with the teachings of the Roberts, et al. patent to provide the corner fill in the hollow in order to establish the seeding material and improve metal contact in the hollow.

Claim 4 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over the Onishi patent in view of newly cited U.S. Patent No. 6,344,413 (Zurcher, et al.). The Examiner acknowledges that the Onishi patent does not disclose that the lower electrode is formed on a surface of a thin film of the same material as that of the lower electrode. However, the Examiner contends that the Zurcher, et al. patent discloses a thin film of titanium which may be deposited on top of the first conductive layer 14, and refers to Column

contends that the Zurcher, et al. patent discloses that the thin film serves as an adhesion layer, at Column 7, lines 7-8. The Examiner concludes, therefore, that it would have been obvious for one with ordinary skill in the art to modify the Onishi structure in accordance with the teaching of the Zurcher, et al. patent to provide a thin film in the lower electrode in order to approve the adhesion to the lower electrode, and further contends that the first conductive layer 14 is made of titanium, which is the same material as the thin film.

Claim 5 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over the Onishi patent in view of U.S. Patent No. 5,767,541 (Hanagasaki). With respect to Claim 5, the Examiner acknowledges that the Onishi patent does not disclose that the top surfaces of the lower electrode and the insulating film are planarized flush with each other. However, the Examiner contends that the Hanagasaki patent discloses a lower electrode which is planarized flush with the insulating film, and refers to Figure 1E of the Hanagasaki patent for showing this. The Examiner further contends that the Hanagasaki patent discloses that planarization could remove surface irregularities, and refers to Column 7, line 37 of the Hanagasaki patent for disclosing this. The Examiner concludes, therefore, that it would have been obvious for one with ordinary skill in the art to modify the Onishi structure with the teaching of the Hanagasaki patent to planarize the top surface of the lower electrode flush with the insulating film in order to remove the surface irregularities.

The comments of the Examiner have been carefully considered. Claim 2 has been cancelled, and Claims 1 and 3 have now been amended to more specifically and clearly define features of Applicant's invention which distinguish over the art of record.

Claim 1 has been specifically amended to define the lower electrode layer as being

portion (e.g., the hollow). This is an important feature of the present invention, as now more specifically defined by amended Claim 1, which reduces the etch time of the ferroelectric memory when compared to conventional ferroelectric memories and, in particular, the semiconductor devices disclosed in the cited references including the Onishi patent, the Roberts, et al. patent, the Zurcher, et al. patent and the Hanagasaki patent.

More specifically, and with particular reference to Figure 2 of the subject application, after the hollow 14 is formed on the first insulation film 12, the first conductive film 26, which is now more specifically defined in amended Claim 1 as being made of the gel dry film, is formed by the sol-gel technique on the surface of the first insulation film 12, including the inside of the hollow 14. This is shown in Figure 2(B) of the drawings. More specifically, a precursor solution is applied to the surface of the first insulation film 12 by the sol-gel technique, and then dried to form the gel dry film. Using the sol-gel technique, the precursor solution that is dripped on the surface of the first insulation film 12 is splashed away due to centrifugal force which occurs in the sol-gel technique. The precursor solution, however, existing inside the hollow 14 will not readily be splashed away. This provides the first conductive film 26 with the film thickness that is greater in the inside of the hollow 14 than over other portions of the ferroelectric memory, as is clearly shown in Figure 2(B). This technique, and the disclosure of the first conductive film 26 as being a gel dry film, and the result that the first conductive film 26 is formed with a film thickness that is greater inside the hollow 14 than outside the hollow 14, are specifically supported by the specification, at Page 6, lines 2-18 thereof.

Because of this, it is now required to etch the total film thickness of the second

application). However, the first conductive film 26 need only be etched at areas that extend out of the hollow 14. As mentioned previously, the portion of first conductive film 26 which extends out of the hollow 14 is thinner than the first conductive film 26 which is inside the hollow 14. Accordingly, the total etch time is reduced, as compared to the etch time in the formation of conventional semiconductor devices in which the entire thickness of the lower electrode of the conventional semiconductor device which is comparable to Applicant's lower electrode 16 would have to be etched. Accordingly, in accordance with the claimed invention, the time during which the film 28 is exposed to the dry-etching plasma atmosphere in order to provide the ferroelectric 18 is reduced. This procedure and the reduction in the etching time resulting from the portion of the first conductive film 26 being thinner outside the hollow 14 than inside the hollow 14 as a result of the lower electrode layer being made of a gel dry film are disclosed in the specification of the subject application, on Page 7, at lines 5-11 thereof. As a result of this structure and procedure, any deterioration of the characteristics of the ferroelectric 18 is prevented or minimized due to the effect of the exposure of the ferroelectric 18 to the plasma, as disclosed on Page 8, lines 1-4 of the subject application.

It is respectfully urged that the Onishi patent does not teach or suggest the structure set forth in now amended Claim 1. More specifically, the Onishi patent does not disclose a lower electrode which is formed as a gel dry film. As clearly shown in Figure 6 of the Onishi patent, the TiN/Ti film 8a and the Pt film 8b are deposited over the entire surface of the interlayer film 7 by a sputtering process or a CVD (chemical vapor deposition) process, as disclosed at Column 8, lines 15-18 of the Onishi patent.

More specifically, the film thickness of the TiN/Ti film 8a and the Pt film 8b on the inside of the contact hole is nearly equal to the film thickness over other portions of the semiconductor memory disclosed in the Onishi patent. This is clearly shown in Figure 6 of the Onishi patent. Accordingly, since the film thickness both inside and outside of the contact hole are nearly equal, the etch time will not be reduced, unlike with the ferroelectric memory of the present invention defined by amended Claim 1, where the lower electrode layer is more specifically defined as being made of a gel dry film. As a result, the characteristics of the ferroelectric layer 9 in the Onishi semiconductor device may be adversely affected due to prolonged exposure to the plasma.

Accordingly, it is respectfully urged that Claim 1, as now amended to specifically define the lower electrode layer as being made of a gel dry film, patentably distinguishes over the Onishi patent and is allowable. It is further respectfully urged that the other references of record, including the Zurcher, et al. patent, the Roberts, et al. patent and the Hanagasaki patent, do not teach or suggest, alone or in combination with the Onishi patent, the structure of the ferroelectric memory now more specifically set forth in amended Claim 1. It is respectfully urged that none of these references discloses a lower electrode layer which is made of a gel dry film in combination with the other elements set forth in Claim 1. Accordingly, it is further respectfully urged that Claim 1, as now more specifically amended, patentably distinguishes over the other references of record and is allowable.

Claim 2 has been cancelled.

Claim 3 has further been amended to more specifically define the ferroelectric memory of the present invention, wherein the first electrode portion is formed by a sol-gel

application, the first electrode portion 16a is formed at the corner of the hollow 14 by a sol-gel technique. This allows the electrode portion 16a to be easily formed specifically at this particular location (that is, in the corner of the hollow 14).

The Roberts, et al. patent was cited in combination with the Onishi patent to suggest the structure of the ferroelectric memory defined by Claim 3 before it was amended herein. It is respectfully urged that neither the Onishi patent nor the Roberts, et al. patent, teaches or suggests, alone or in combination, that the first electrode portion is formed by a sol-gel technique only at a corner of the hollow.

More specifically, and as shown in Figure 3 of the Roberts, et al. patent, the conductive corner fill 32 at the lower corner 30 of the contact 20 is not formed by a sol-gel technique, but rather is formed by a sputter deposition using the upper corner 26 of the first conductive layer 14 as the sputter deposition target. This is clearly disclosed in the Roberts, et al. patent, at Column 6, lines 40-45 thereof. Accordingly, the conductive corner fill 32 is urged to be more difficult to form using this technique than using the sol-gel technique of the invention defined by amended Claim 3. Such structure, as now more specifically defined by amended Claim 3, is not found in either the Onishi patent or the Roberts, et al. patent, nor is there any disclosure to form a first electrode portion by a sol-gel technique only at a corner of a hollow in a semiconductor device in any of the other references of record, including the Zurcher, et al. patent and the Hanagasaki patent. Accordingly, it is respectfully urged that Claim 3, as now more specifically amended, patentably distinguishes over the references of record and is allowable.

Claim 4 has been rejected as being obvious in view of the Onishi patent and the Zurcher, et al. patent. The structure of the ferroelectric memory defined by Claim 4 is shown, by way of example, in Figure 8 of the drawings.

As shown in Figure 8, the thin film 36 is formed on the surface of the planarized first conductive film 26 by using the same material as that of the planarized first conductive film 26. This is done to eliminate surface roughening in the first conductive film 26 due to the planarization process, and reference is respectfully made to Page 9, lines 17-20 of the subject application for disclosing this structure and the advantages of such. It should be noted that the thin film 36 does not serve as the adhesion layer, but rather serves as the layer to eliminate surface roughening.

Contrary to the teachings of the present invention and the structure of the ferroelectric memory set forth in Claim 4, the semiconductor device disclosed in the Onishi patent has no layer made of the same material as the lower electrode 8 formed between the lower electrode 8 and the ferroelectric film 9. This is clearly shown in Figure 6 of the Onishi patent. Thus, the Onishi patent does not teach or suggest the particular structure set forth in Claim 4 of the subject application.

The Zurcher, et al. patent does not supplement the inadequacies of the Onishi patent in teaching or suggesting the ferroelectric memory defined by Claim 4. In particular, the Zurcher, et al. patent does not disclose that the thin film of titanium is deposited on top of the first capacitor layer 70. In particular, the Zurcher, et al. patent only discloses that the first capacitor electrode layer 210 is separated from the second capacitor electrode layer 244 by way of the capacitor dielectric layer 242, as shown in Figure 15 and as disclosed at Column

patent does not disclose the specific structure of the ferroelectric memory set forth in Applicant's Claim 4. Thus, it is respectfully urged that Claim 4 patentably distinguishes over the Onishi patent, and the Zurcher, et al. patent, each either taken alone or combined with the other, and is allowable.

Claim 5 has been rejected as being obvious in view of the Onishi patent and the Hanagasaki patent. The rejection of Claim 5 as being obvious in view of these two reference is respectfully traversed.

The structure the ferroelectric memory defined by Claim 5 is shown, by way of example, in Figure 7 of the subject application. As shown in Figure 7, the film 28 is formed after planarizing the top surfaces of the first conductive film (i.e., the lower electrode) 26 and the insulation film 12 so that the two will be flush with each other. As a result, the lower electrode 16 is entirely buried in the hollow 14. As such, the etch time can be further shortened, as it is unnecessary to etch that portion of the first conductive film 26 which extends out of the hollow 14 in the later process. This structure, and the advantages of such, are specifically disclosed at Page 9, lines 14-17 of the subject application.

The Examiner acknowledges that the Onishi patent does not disclose the top surfaces of the lower electrode and the insulating film being planarized flush with each other, but contends that the Hanagasaki patent discloses the lower electrode is planarized flush with the insulating film, and refers to Figure 1E of the Hanagasaki patent as disclosing this. However, with reference to Figure 1E of the Hanagasaki patent, the lower electrode is not denoted by the reference number 8 in Figure 1E, but rather by the reference numeral 9a in Figure 1G of the Hanagasaki patent. Reference numeral 8 refers to the W plug (please see Column 7, line

disclose that the upper surface of the lower electrode 9a and the surface of the insulating layer are flush with each other, as specifically set forth in Applicant's Claim 5.

Furthermore, even if the Onishi patent and the Hanagasaki patent were combined with each other, the etch time in forming such a hypothetical semiconductor device cannot be shortened as it is in the presently claimed invention, because it is still necessary to etch the portion of the first conductive film 26 which extends out of the hollow 14 in the later process. Accordingly, it is respectfully urged that Claim 5 patentably distinguishes over the Onishi patent and the Hanagasaki patent, each reference taken alone or in combination with each other, and further patentably distinguishes over each of the other references cited but not applied against Claim 5.

In view of the foregoing amendments and remarks, entry and favorable consideration of the amendments to Claims 1 and 3, reconsideration of Claims 4 and 5 and allowance of the application with Claims 1 and 3-5 are respectfully solicited.

Respectfully submitted,

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